ESD Protection Diodes

1KE1G3V0 ~ 1KE1G5V0

SOD-523

Top View

PIN DESCRIPTION

PIN	DESCRIPTION
1	Cathode
2	Anode

■ Features

- ● Low Clamping Voltage.
- ● Small Body Outline Dimensions..
- ● Low Leakage
- ● ESD Rating of Class 3(>16kV) per Human Body
- ● IEC61000-4-2 Level 4 ESD Protection IEC61000-4-4 Level 4 EFT Protection

■ Absolute Maximum Ratings Ta = 25℃

Parameter		Symbol	Value	Unit
IEC 61000-4-2(ESD)	Contact		±30	KV
	Air		±30	
IEC 61000-4-4(EFT)			40	A
ESD Voltage	Per Human Body Model		16	KV
Total Power Dissipation on FR-4 Board *1		P_D	500	mW
Junction Temperature		TJ	150	℃
Storage Temperature range		Tstg	-55 to +150	
Lead Solder Temperature - Maximum (10 Second Duration)		TL	260	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

*1. FR−4 printed circuit board, single−sided copper, mounting pad 1 cm^2

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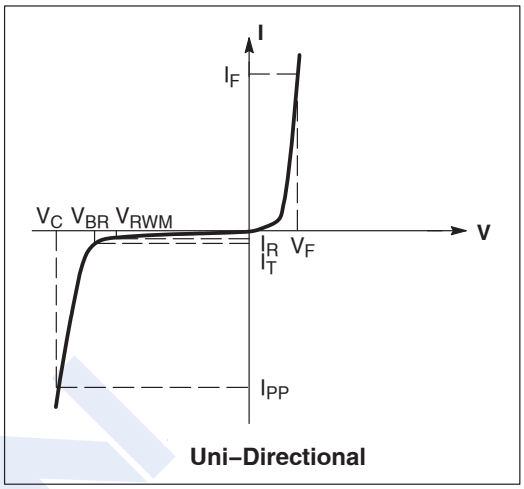
■ Electrical Characteristics Ta = 25℃ unless otherwise noted

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_F	Forward Current
V_F	Forward Voltage @ I_F
P_{pk}	Peak Power Dissipation
C	Max. Capacitance @V_R = 0 and f = 1 MHz



Uni–Directional

■ Electrical Characteristics Ta = 25℃

Device**	Device Marking	V_{RWM} (V)	I_R (μA) @ V_{RWM}	V_{BR} (V) @ I_T (Note 2)	I_T	V_C (V) @ I_{PP} = 5.0 A†	V_C (V) @ Max I_{PP}†	I_{PP} (A)†	P_{pk} (W)†	C (pF)
		Max	Max	Min	mA	Typ	Max	Max	Max	Typ
1KE1G3V0	Z5	3.0	0.05	4.0	1.0	7.5	12.9	11.0	137	125
1KE1G3V3	ZE	3.3	0.05	5.0	1.0	8.4	14.1	11.2	158	105
1KE1G5V0	ZF	5.0	0.05	6.2	1.0	11.6	18.6	9.4	174	80

**Other voltages available upon request.

1.Surge current waveform per Figure5.

2.VBR is measured with a pulse test current IT at an ambient temperature of 25 ℃

3.For test procedure see Fugures 3 and 4.

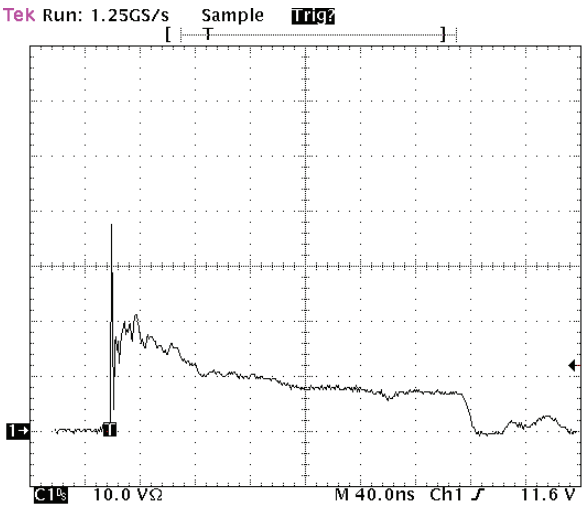


Figure 1. ESD Clamping Voltage Screenshot
Positive 8 kV contact per IEC 61000−4−2

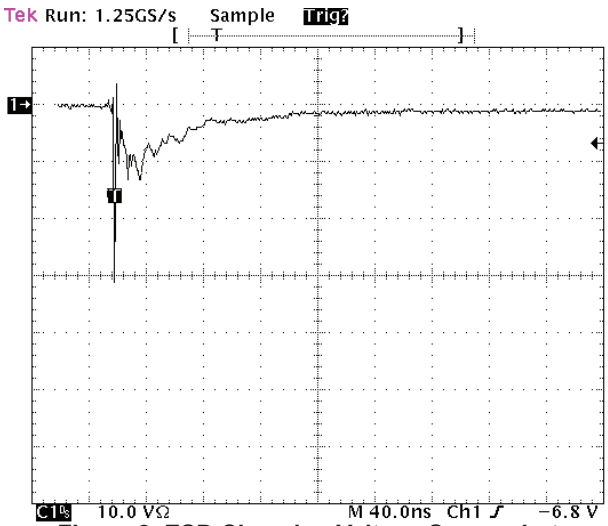


Figure 2. ESD Clamping Voltage Screenshot
Negative 8 kV contact per IEC 61000−4−2

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IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

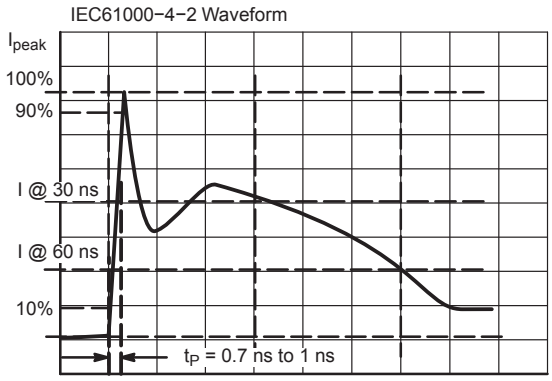

Figure 3. IEC61000−4−2 Spec

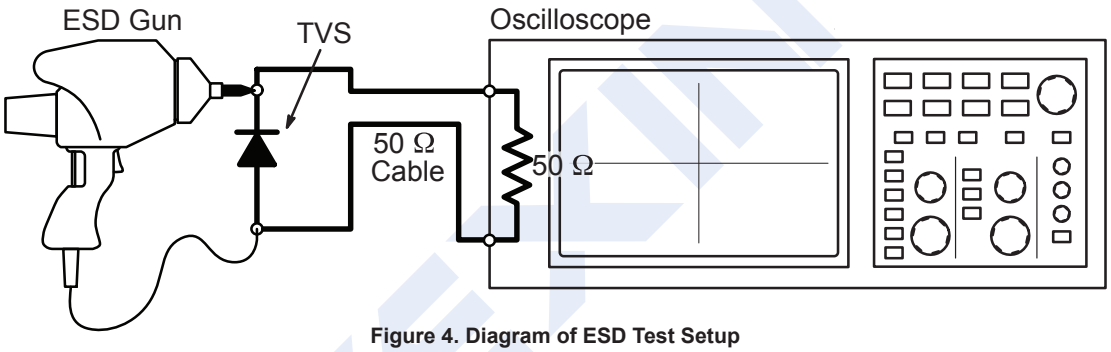

Figure 4. Diagram of ESD Test Setup

ESD Voltage Clamping

For sensitive circuit elements ,it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level.

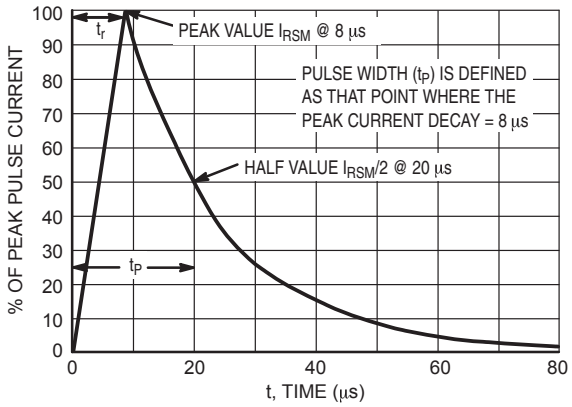

Figure 5. 8 X 20 μs Pulse Waveform

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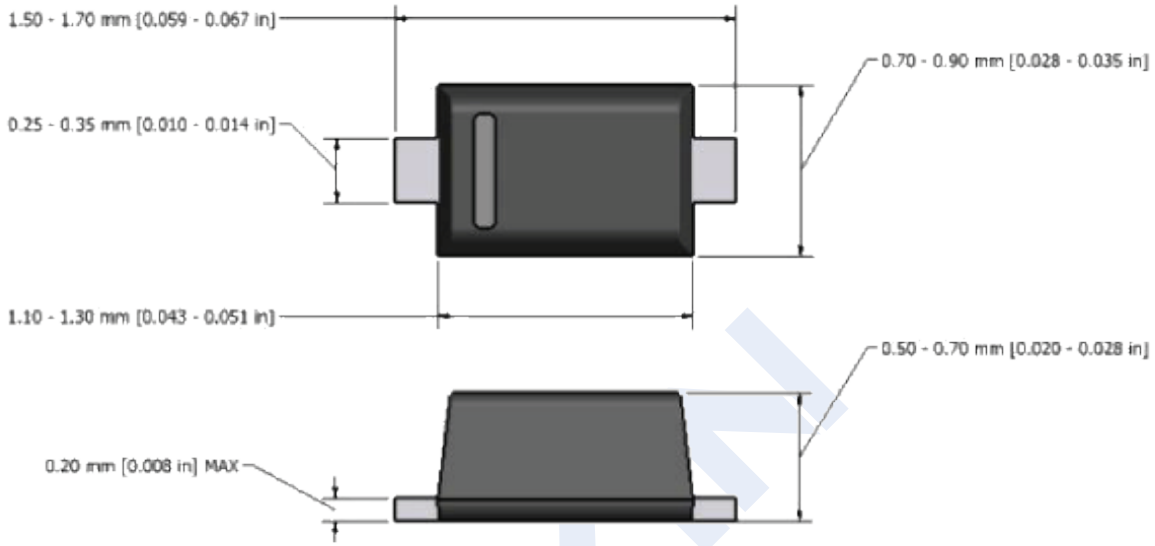
■ Package Outline Dimensions (SOD-523)



Note: Dimensions are exclusive of Burrs, Mold Flash & Tie Bar extrusions.

■ The Recommended Mounting Pad Size